## REMARKS

This Amendment responds to the final Office Action mailed January 13, 2006 in the above-identified application. A Request for Continued Examination (RCE) accompanies this Amendment. In view of the foregoing amendments, allowance of the application is respectfully requested.

Claims 1, 4-6, 30, 32-33, 36, 39 and 41 were previously pending in the application. Claims 8-29 and 43-45 were withdrawn from consideration, and claims 2-3, 7, 31, 34, 35, 37-38, 40 and 42 were previously cancelled. By this Amendment, claims 1, 6, 30, 36 and 41 are amended. Withdrawn claims 8-29 and 43-45 are cancelled without prejudice or disclaimer. Accordingly, claims 1, 4-6, 30, 32-33, 36, 39 and 41 are pending for examination. Claims 1, 6, 30, 36 and 41 are independent claims. No new matter has been added.

The Examiner has rejected claims 1, 6, 30, 36, 39 and 41 under 35 U.S.C. §103(a) as unpatentable over Sakai (US 6,131,143) in view of Hanawa et al. (US 6,282,505). Claims 4-5 and 32-33 are rejected under 35 U.S.C. §103(a) as unpatentable over Sakai in view of Hanawa et al., and further in view of Liao et al. (US 6,857,061). The rejections are respectfully traversed in view of the amended claims.

Sakai discloses a multi-way associative cache memory. The cache memory shown in Fig. 1 includes a decoder 1, first tag memory 2, second tag memories 3a, ..., 3n, multi-way data memories 5a, ..., 5n, comparators 6, 7a, ..., 7n and way selector 9 (col. 4, lines 25-28). Tag memory 2 stores high order bits of an address tag and tag memories 3a, ..., 3n store lower order bits of the address tag (col. 4, lines 29-32). The high order address tag and the low order address tag of address 10 are compared with the contents of tag memories 2 and 3a, ..., 3n by comparators 6 and 7a, ..., 7n, respectively (col. 4, line 36 to col. 5, line 15).

Hanawa discloses a multi-port memory subdivided into a plurality of memory banks, each of the memory banks including means for storing therein data and an address of the data (col. 2, lines 47-50). An address from a first memory port is input to a first memory bank in a first cycle and a comparison is made to determine whether the data to be accessed is stored in the first memory bank.

If the data is stored in the first memory bank, the data is accessed. If the data is missing, the address is input to a second memory bank in a second cycle and a comparison is made to determine whether the data to be accessed is stored in the second memory bank (col. 3, lines 22-34). The two memory banks can be accessed simultaneously (col. 3, lines 46-52), but different ways in the same memory bank cannot be accessed simultaneously.

Independent claims 1, 6, 30, 36 and 41 have been amended to recite an associative cache including a plurality of tag memory locations for storing addresses and a plurality of data memory locations for storing data. The memory locations are organized as two or more ways, and the data memory location in first and second ways can be accessed concurrently by first and second devices, respectively.

Sakai and Hanawa, taken individually or in combination, do not disclose or suggest an associative cache wherein *data memory locations in first and second ways can be accessed concurrently by first and second devices*, as claimed. In Sakai, one of the data memories 5a, ..., 5n is selected by way selector 9. "Way selector 9 selects *one* of data stored in data memories 5a, ..., and 5n corresponding to hit signals received from comparators 6, 7a, ..., and 7n" (col. 4, lines 40-42 – emphasis added). In Hanawa, data cache 430 shown in Fig. 1 includes two memory banks 125 and 135, each of which is two-way set associative (col. 5, lines 55-56; col. 6, lines 8-9; and col. 6, lines 26-28). If there is a hit in one of the memory banks, data corresponding to the matching way is selected by a selector and read from the corresponding memory array (col. 6, lines 18-24 and col. 6, lines 36-43). In Hanawa, data from *one* of the ways in each associative cache can be accessed at a given time. Thus, both Sakai and Hanawa disclose associative caches wherein the data in a single way is accessed. By contrast, Applicant's claims are directed to an associative cache wherein data memory locations in first and second ways are accessed concurrently by first and second devices. Accordingly, Applicant's amended claims are clearly and patentably distinguished over Sakai in view of Hanawa, and withdrawal of the rejection is respectfully requested.

Independent claims 1, 6, 30, 36 and 41 have been amended to include limitations similar to those discussed above. Accordingly, independent claims 1, 6, 30, 36 and 41 are clearly patentable over Sakai in view of Hanawa for the same reasons. Claims 4 and 5 depend from claim 1, claims 32 and 33 depend from claim 30, and claim 39 depends from claim36. Claims 4-5, 32-33 and 39 are patentable over Sakai in view of Hanawa for at least the reasons discussed above in connection with claims 1, 6, 30, 36 and 41. The Liao patent does not provide the teachings that are lacking in Sakai and Hanawa. Accordingly, claims 1, 4-6, 30, 32-33, 36, 39 and 41 are in condition for allowance.

## CONCLUSION

A Notice of Allowance is respectfully requested. The Examiner is requested to call the undersigned at the telephone number listed below if this communication does not place the case in condition for allowance.

If this response is not considered timely filed and if a request for an extension of time is otherwise absent, Applicant hereby requests any necessary extension of time. If there is a fee occasioned by this response, including an extension fee, that is not covered by an enclosed check, please charge any deficiency to Deposit Account No. 23/2825.

Respectfully submitted,

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